VSC8211 Evaluation Board

User Guide

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Vitesse Proprietary

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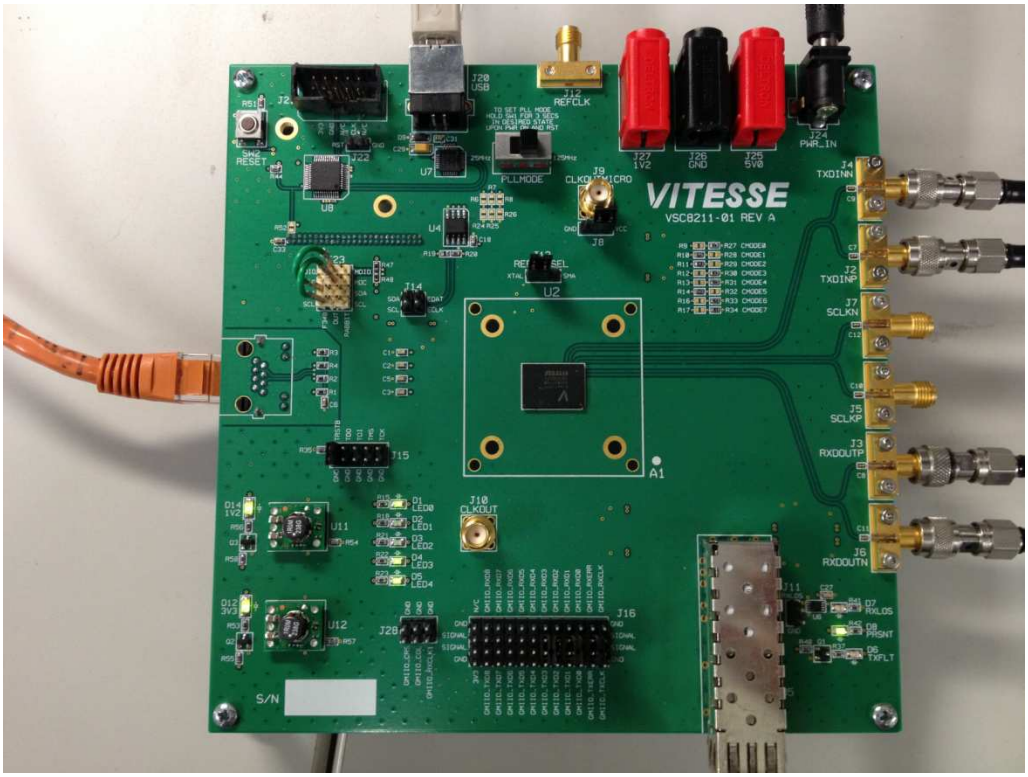
Revision	Date	Description
Rev 1.0	December 18, 2013	First release

1 Introduction

The VSC8211 device is a low-power, Gigabit Ethernet transceiver suited for Media Converters and Ethernet Switches with virtually any serial or parallel MAC interface. The VSC8211 device also includes Vitesse's VeriPHY Cable Diagnostics feature.

This document describes the operation of the VSC8211 Evaluation Board (VSC8211EV). The Quick Start section describes how to install and run the graphical user interface (GUI) to fully control the evaluation board.

Figure 1. VSC8211EV



The following reference documents provide additional information about the operation of the VSC8211 evaluation board.

- VSC8211 Datasheet
  (https://www.vitesse.com/products/download.php?fid=118&number=VSC8211)
- VSC8211 Evaluation Board GUI
  (https://www.vitesse.com/products/download.php?fid=5157&number=VSC8211)
- VSC8211 Evaluation Board Schematics
  (https://www.vitesse.com/products/product.php?number=VSC8211)

2 General Description

The VSC8211EV provides the user a way to evaluate the VSC8211 device in multiple configurations. One RJ-45 connector is provided for the copper media interface. The MAC interface is accessible via SMA connectors. An SFP cage is available for serial to serial configurations, and headers are available for the parallel interface

The VSC8211's internal registers are accessed via the MDIO bus from an external microcontroller driven by an external PC via USB. The accompanying GUI enables the user to read and write the device registers. Alternatively, the VSC8211EV also has the capability to configure the VSC8211 through an EEPROM or Rabbit microcontroller (not-provided).

The evaluation board has the option to use VSC8211's internal on-chip oscillator by connecting a 25MHz crystal to XTAL1 and XTAL2 or an external reference clock signal through the REFCLK SMA (J12).

2.1 Hardware Features

2.1.1 Power Connections

For convenience, the evaluation board runs off a single +5VDC power supply. On board DC-DC convertors create the +3.3VDC rail for the board and optional +1.2VDC rail. Power is supplied to the upper right corner of the board. Power can be applied either to the 5.5 x 2.1 mm barrel connector (J24) or the banana receptacles (J25 and J26). J27 is an optional monitor point for the 1.2V rail. When powered by a bench top supply the board may draw up to 3A maximum, module included.

2.1.2 Copper Port RJ45 Connections

The RJ45 copper media PHY port (J1) uses a generic RJ45 jack with a discrete Pulse H5008 magnetic transformer.

2.1.3 SGMII MAC Interface via SMA

The serial MAC interface is available through SMA connectors (J2, J4, J3, and J6), including the optional SCLK (on J5 and J7).

2.1.4 GMII, RGMII, MII, TBI and RTBI MAC Interface

The parallel MAC interfaces are available through pin headers on J16 and J28.

2.1.5 Fiber Transceiver Interface (SFP Cage)

The Fiber transceiver differential pair used in the SGMII to SerDes PHY operating mode is supported with the standard SFP cage (U5).

2.1.6 Switches

Switch SW1 allows the user to select the mode of the EECLK/PLLMODE pin. In the on position a logic high voltage (pull-up resistor) configures the device for a 125MHz reference clock while a logic low voltage (pull-down resistor) selects a 25MHz reference clock option. This is a momentary ON switch which requires the user to hold it in the on position for 3 seconds during board power up or device reset.

2.1.7 Taitien 25MHz Crystal

The evaluation board is shipped configured to use the VSC8211's internal on-chip oscillator. The jumper on J13 should be installed in the XTAL (left) position, and the jumper on J8 should be installed in the PLL enable or VCC (right) position.

Note Review the required action for SW1 mentioned above.

2.1.8 External RefClk Option

The user may choose to provide an external PHY REFCLK via the SMA connector (J12). The user must configure the device by installing a jumper on J8 in the PLL disable or ground (left) position and installing a jumper on J13 in the SMA (right) position.

2.1.9 Silabs Microcontroller

A Silabs F340 microcontroller is included to facilitate a software interface to the registers on the VSC8211 through a USB port.

To communicate to the EEPROM or to use a Rabbit microcontroller rather than the Silabs F340, install jumpers on J23 and J14 accordingly.

Note A silk-screen error exists on the PCB for J23 such that the MDIO and MDC signals are swapped with the SDA and SCL signals respectively for the F340 and Rabbit signals. Refer to Figure 2 for clarity of the default configuration.

Figure 2. MDIO/MDC Jumpers on J23 to SiLabs F340 pins



2.1.10 EEPROM Option

The user may choose to configure theVSC8211 via an EEPROM load. In order to program the EEPROM properly, pull-up or pull-down resistors must be configured for either R6 – R8 or R24 – R26. Please refer to Section 19 of the datasheet regarding to EEPROM programming requirement.

2.1.11 CMODE Pins (Pin-Strap mode)

On the upper right of the board, there is an option to change the CMODE pin pull-up or pull-down resistors, R9 - R17 and R27-R34. Please refer to Section 18 of the datasheet for the detail on how to program the desired operating condition parameters through the CMODE configuration bits and how to choose the value of each CMODE pull-up or pull-down resistor.

2.1.12 LED Interface

LED1 to LED5 are available on the lower left of the board. Please refer to Section 14 of the datasheet for details regarding how to configure the LEDs.

2.1.13 CLOCKOUT SMA

The user should observe a 125MHz output clock through this SMA if the internal PHY PLL is operating properly.

2.2 Software Requirements

The VSC8211 GUI can be loaded on to any PC or laptop that complies with the following requirements:

1. The PC must run a recent version of MS-Windows. According to the Microsoft website, the following operating systems can run .NET based applications:

- Windows 2000
- Windows XP
- Windows Vista
- Windows-7

Note The GUI may be slower when run on Windows 2000 operating system.

2. Hardware requirements must be considered when deploying/installing .NET applications. The minimum hardware requirement for a system running a .NET application is a Pentium 90MHz with 32 MB of RAM. For best performance, a newer system is recommended along with a minimum of 1 GB of RAM.
3. If the .NET Framework 2.0 is not already installed, it may be obtained from the following link: http://www.microsoft.com/downloads/details.aspx?FamilyID=0856EACB-4362-4B0D-8EDD-AAB15C5E04F5&displaylang=en

3 Quick Start

3.1 Board Configuration

Prior to powering the board, ensure that the jumpers and switches are in the following positions.

Table 1. Switch and Jumper Configuration

Switch/Jumper	Position
J23 (MDC)	Jumper installed connecting DUT MDC to F340 SCL **NOTE**: This is due to a layout error on the PCB. Refer to Section 2.1.9 for additional details.
J23 (MDIO)	Jumper installed connecting DUT MDIO to F340 SDA **NOTE**: This is due to a layout error on the PCB. Refer to Section 2.1.9 for additional details.
J15 (TRSTB)	Jumper installed connecting to GND. This is not required when R35 is installed.
J13 (XTAL1/REFCLK)	Jumper installed connecting center pin to XTAL.
J8 (PLL ENABLE/DISABLE)	Jumper installed connecting center pin to PLL ENABLE.
SW1	Hold in the left position during power-up and reset.

3.1.1 Power Up

Provide +5VDC to the board by plugging in the power cable (included in the kit) to J24. Two green LEDs should illuminate: D12 on the left side of the board indicating +3.3VDC present, and D14 indicating +1.2VDC present.

3.1.2 Clock and Reset

Power must be applied and the clock (either 25MHz or 125MHz) must be active at the correct frequency for the prescribed period of time in the datasheet before the RESETB pin is released. PLLMODE and OSCDISB pins are sampled during the device power-up or on assertion of RESETB pin.

The board will be shipped configured for use of the 25MHz crystal thus OSCDISB must be pulled up and PLLMODE must be pulled down during power-up or assertion of RESETB by setting J8 to the PLL enable position and holding SW-1 in the 25MHz position upon power-up.

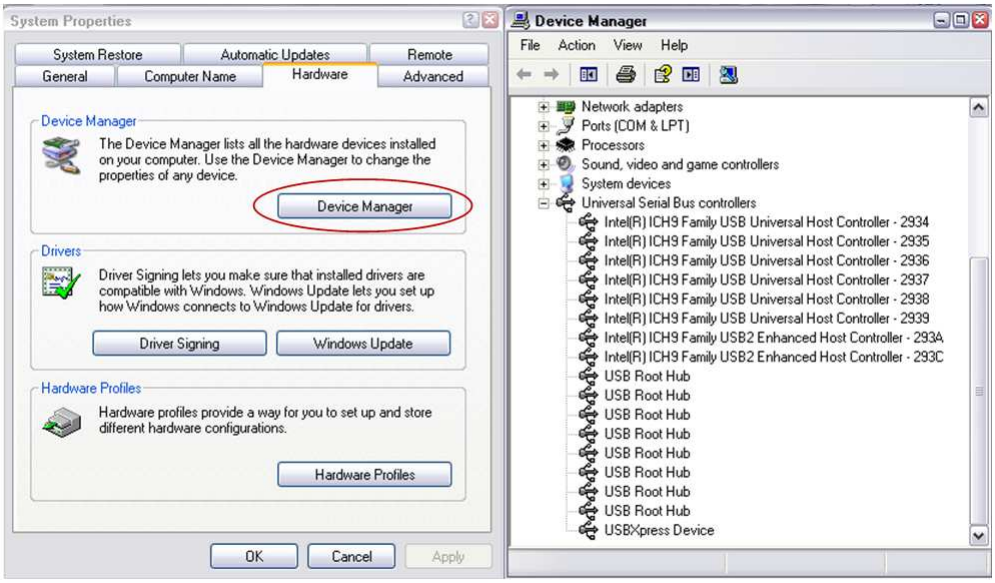
3.2 GUI and Driver Installation

Download the VSC8211EV GUI from Vitesse's website onto a PC that has a USB port. Install the GUI by launching the setup.exe file. Once installed, connect the USB cable between the USB port of the PC and the USB connector (J20) on the evaluation board. Ensure the MDIO and MDC jumpers are properly placed from DUT to F340 on J23 to establish the connection between the VSC8211's SMI pins and the SiLab F340.

USB communication is assisted by the Silabs USBXpress® drive. If not present on the PC, the user will need to download the USBXpress Development Kit from the Silicon Labs website (URL: http://www.silabs.com/products/mcu/Pages/USBXpress.aspx). Follow the installation directions after downloading the development kit.

To ensure the USBXpress driver is installed and properly recognizing the evaluation board, go to Control Panel and click on System>Hardware>Device Manager, and inspect the Universal Serial Bus controllers listed to see if "USBXpress Device" appears. Figure 3 shows that the PC recognizes that a USBXpress Device is connected.

Figure 3. USBXpress as Seen From the Device Manager Window



3.3 Using the GUI

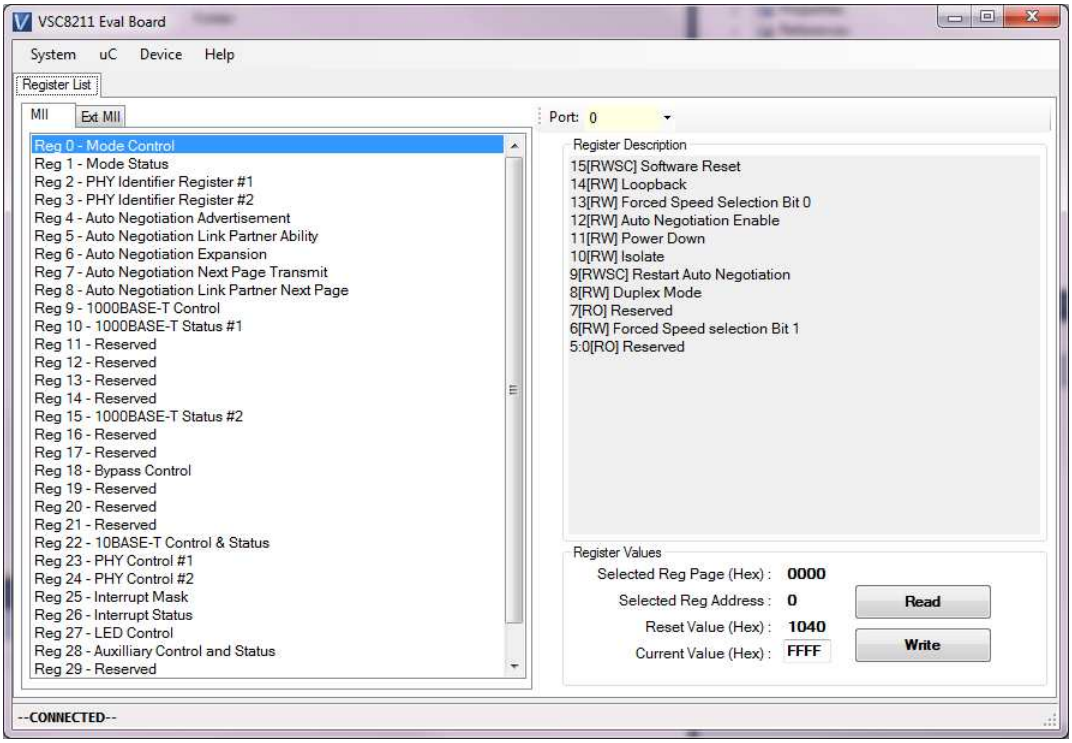
Launch the GUI either by clicking on the Desktop shortcut or clicking on the "Start – Programs – Vitesse Semiconductor Corp - VSC8211_Evaluation_System" icons. The initial window will detect the attached USB devices automatically. Figure 4 shows a typical EVB Connection window.

Figure 4. Connection Window



The EVB serial number should appear. If not, click on "Scan For USB Devices." Select that EVB serial number then click "Launch GUI". The Register List window will appear as shown in Figure 5.

Figure 5. Register List Window



Verify that the device is up and running by reading MII Register 0. It should read back 0x1040. Reading back "0000" or "FFFF" (all 0's or all 1's) indicates a problem.

To read or write the extended MII registers click on the ExtMII tab.

An initialization script may be used to configure multiple VSC8211 registers. The initialization script is simply a text file which contains a list of registers to be written. Select the Device item on the top pull down menu area and click on Load-All-Registers option. A pop-up window will appear. Navigate to and select the desired script to be loaded.

As per Section 31.1 of the datasheet, there are a number of internal registers that must be changed from their default value during device initialization. Use this method to initialize the device by loading "vsc8211_workaround33_1.txt" included in the GUI package under the Script/ directory. GUI Setup

3.4 Test Cases

3.4.1 CAT5 to SGMII with Clause 37 AutoNeg Enabled

After power-up or reset, VSC8211 as configured on the evaluation board will operate according to CAT5 to SGMII with Clause 37 Auto Negotiation enabled. The 1G Ethernet received at the RJ-45 port is routed through the VSC8211 and looped back via SGMII through SMA cables.

1. Set up the copper Ethernet traffic source (e.g., IXIA or Smartbits)
2. Connect an Ethernet cable to an RJ-45.
3. Loopback SGMII RXDOUT to TXDIN via SMA cables.
4. Monitor the link-up bit in MII Register 1, bit 2 (MII 1.2), read twice to update. Traffic should now be flowing.

3.4.2 CAT5 to RGMII

1. Set up the copper Ethernet traffic source (e.g., IXIA or Smartbit) and connect a CAT5e cable to the RJ-45.
2. Loopback the RGMII signals using 0-ohm header jumpers on J16.
3. Write 0x1824 to MII Register 23 (Port 0, PHY Control #1). This also sets the internal RGMII TXC skew to 2.0ns for this board.
4. Write 0x9040 to MII Register 0 (Port 0, SW Reset for PHY Control setting to take effect).
5. Monitor the link-up bit in MII Register 1, bit 2 (MII 1.2), read twice to update. Traffic should be flowing.

3.5 Useful Registers

3.5.1 Ethernet Packet Generator

ExtMII 29E is the Ethernet Packet Generator register. Refer to datasheet for configuration options.

A bad-CRC counter is in ExtMII 23.7:0. This counter will be saturate at 0xFF and is cleared when read.

3.5.2 Far-End Loopback

When MII Register 23 bit 3 is set to 1, it forces incoming data from a link partner on the media side to be retransmitted back to the link partner on the media interface.

3.5.3 Near-End Loopback

When MII Register 0 bit 14 is set to 1, the transmit data (TDP/TDN) on the MAC side is looped back onto the receive data (RDP/RDN pins) to the MAC.

4 Additional Information

For any additional information or questions regarding the devices mentioned in this document, contact your local sales representative.